17. (original) In a computer system having a source computer and a destination computer having a clock that regulates timing of activities at the destination computer, a method comprising the steps of:

providing a logical structure for encapsulating multiple streams of data, said streams of data being stored in packets;

storing clock licenses that dictate advancement of a clock in multiple ones of the packets;

transmitting the logical structure from the source computer to. the destination computer; and

for each packet that holds a clock license, advancing the clock at the destination computer as dictated by the clock license in response to receiving the packet at the destination computer.

18. (currently amended) The method of claim 4317 wherein each clock license includes a time value to which the clock at the destination computer is to be advanced.

19. (original) The method of claim 18 wherein each clock license includes an expiration time after which the clock license is invalid.

37. (previously amended) In a computer system, a computer-readable storage medium holding a logical structure that encapsulates components comprising:

multiple streams of data wherein the streams of data are stored in packets;

clock licenses that each dictate advancement of a clock that regulates rendering of the data in the packets.

38. (currently amended) The computer-readable storage medium of claim ~~5337~~ wherein each clock license includes a time value to which the clock at the destination computer is to be advanced.

39. (original) The computer-readable storage medium of claim 38 wherein each clock license includes an expiration time after which the clock license is invalid.

42. (previously amended) A data processing system comprising:

a source computer with a storage;

a logical structure stored in storage for encapsulating multiple data streams, data from said data streams being incorporated in packets;

a clock license being encapsulated into at least one packet for advancing a clock at a destination when processed at the destination.

43. (currently amended) In a computer system having a source computer and a destination computer having a clock that regulates timing of activities at the destination computer, a ~~The~~ method ~~as defined in Claim 17, wherein: the~~ comprising the steps of:

providing a logical structure for encapsulating multiple streams of data, said streams of data being stored in packets, ~~comprises:~~ by:

storing samples of data from multipl data streams in the packets;

storing replicas of information in at least some of the packets;

storing error correcting data in the at least some of the packets, wherein the error correcting data identifies an error correcting method for the at least some of the packets;

setting a flag in the packets that hold the replicas; and

encapsulating the packets into the logical structure, wherein at least some of the packets hold the replicas;

storing clock licenses that dictate advancement of a clock in multiple ones of the packets;

transmitting the packets of the logical structure on a packet-by-packet basis over a packet switched network from the source computer to the destination computer; and

for each packet that holds a clock license, advancing the clock at the destination computer as dictated by the clock license in response to receiving the packet at the destination computer. ~~wherein: the method further comprises transmitting the packets of the logical structure on a packet-by packet basis over a packet switched network from the source computer to the destination computer.~~

44. (previously added) The method as defined in Claim 43, wherein the replicas of information hold property information regarding the samples of data.

45. (previously added) The method of claim 43 wherein portions of a sample are stored in selected packets and a replica of property information regarding the sample is stored in each packet in which a portion of the sample is stored.

46. (previously added) The method of claim 43, further comprising the step of examining one of the replicas of information at the destination computer when one of the packets is lost during the transmitting.

47. (previously added) The method of claim 43, further comprising using the error correcting data in the at least some of the packets to correct an error when the transmitted logical structure is received at the destination.

48. (previously added) The method of claim 43, wherein:

the logical structure includes a header section and a data section; and

the error correcting data is stored in multiple packets in the data section.

49. (previously added) The method of claim 48, wherein information in the header section of the logical structure indicates what error correcting methodology is used with the error correcting data stored in the multiple packets in the data section.

50. (previously added) The method of Claim 48, wherein the header section holds information regarding multiple error correcting methods.

51. (previously added) The method of claim 43, wherein the error correcting data identifies one of a plurality of error correcting methods.

52. (previously added) The method of claim 43, wherein the error correcting data holds parity bits.

53. (currently amended) In a computer system, a ~~The~~ computer-readable storage medium ~~as defined in claim 37~~ holding a logical structure that encapsulates components comprising:

multiple streams of data wherein the streams of data are stored in packets; and

clock licenses that each dictate advancement of a clock that regulates rendering of the data in the packets, wherein:

the streams of data stored in the packets are samples of data from multiple data streams in packets for transmission on a packet-by-packet basis over a packet switched network;

replicas of information are stored in at least some of the packets;

error correcting data is stored in the at least some of the packets;

the error correcting data identifies an error correcting method for the at least some of the packets; and

a flag is stored in each said packet that holds the replicas.

54. (previously added) The computer-readable storage medium of claim 53 wherein portions of a sample are stored in selected packets and a replica of property

information regarding the sample is stored in each packet in which a portion of the sample is stored.

55. (previously added) The computer-readable storage medium as defined in claim 53, wherein:

the logical structure includes a header section and a data section, and

the error correcting data is stored in multiple packets in the data section.

56. (previously added) The computer-readable storage medium as defined in claim 55, wherein the information in the header section of the logical structure indicates what error correcting methodology is used with the error correcting data stored in the multiple packets in the data section.

57. (previously added) The computer-readable storage medium as defined in claim 56, wherein the header section holds information regarding multiple error correcting methods.

58. (previously added) The computer-readable storage medium as defined in claim 53, wherein the error correcting data identifies a plurality of error correcting methods.

59. (previously added) The computer-readable storage medium as defined in claim 53, wherein the error correcting data holds parity bits.

60. (currently amended) A ~~The~~ data processing system ~~as defined in claim~~ 42 comprising:

a source computer with a storage;

a logical structure stored in the storage for encapsulating multiple data streams, data from said data streams being incorporated in packets; and

a clock license being encapsulated into at least one packet for advancing a clock at a destination when processed at the destination, wherein:

the streams of data stored in the packets are samples of data from multiple data streams in the packets for transmission on a packet-by-packet basis over a packet switched network;

replicas of information are stored in at least some of the packets;

error correcting data is stored in the at least some of the packets;

the error correcting data identifies an error correcting method for the at least some of the packets; and

a flag is stored in each said packet that holds the replicas.

61. (currently amended) A ~~The~~ data processing system ~~as defined in claim~~ 42 comprising:

a source computer with a storage;

a logical structure stored in storage for encapsulating multiple data streams, data from said data streams being incorporated in packets; and

a clock license being encapsulated into at least one packet for advancing a clock at a destination when processed at the destination, wherein portions of a sample are stored in selected packets and a replica of property information regarding the sample is stored in each packet in which a portion of the sample is stored.

62. (currently amended) The data processing system as defined in claim 6042, wherein:

the logical structure includes a header section and a data section, and

the error correcting data is stored in multiple packets in the data section.

63. (previously added) The data processing system as defined in claim 62, wherein information in the header section of the logical structure indicates what error correcting methodology is used with the error correcting data stored in the multiple packets in the data section.

64. (previously added) The data processing system as defined in claim 63, wherein the header section holds information regarding multiple error correcting methods.

65. (currently amended) The data processing system as defined in claim 6042, wherein the error correcting data identifies a plurality of error correcting methods.

66. (currently amended) The data processing system as defined in claim 6042, wherein the error correcting data holds parity bits.